TG7200C Datasheet

DS-TG7200C-E01 V1.0

2023/10/18

Contents

1. Features

Wi-Fi

- IEEE 802.11 b/g/n 1x1 compliant
- Supports 20 MHz channel
- STBC supported
- Working mode STA, AP, Direct
- Concurrent AP + STA
- TX power up to +19 dBm
- RX sensitivity -99 dBm

Bluetooth Low Energy

- Bluetooth 5.2 Low Energy (LE)
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Advertising extensions
- Bluetooth direction finding: Angle of Arrival (AoA) and Angle of Departure (AoD)
- Supports an antenna array with up to 16 antennas for precise positioning

Core

- 32-bit MCU at up to 160 MHz
- UART Flash download
- JTAG debug interface

Memory

- 2 MB SiP Flash
- 288 KB RAM
- 4-byte eFuse

Clock Management

- External oscillator: 26 MHz crystal oscillator (XTALH)
- Internal oscillator: 26–160 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 480 MHz DPLL

Power Management

- 2.7 to 3.6 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded LDO regulators
- Low power consumption:
  - Active mode RX: 30 mA
  - Normal sleep mode: 300 µA
  - Low-voltage sleep mode: 75 µA
  - Shutdown mode: 0.5 µA

Peripherals

- 19 GPIOs
- 1x SPI
- 2x UART: 1 with Flash download support
- 1x I2C
- 1x general-purpose DMA controller (GDMA) with 6 channels
- 6x 32-bit PWM channel
- 10-bit AUX ADC, up to 6 channels
- 6x general-purpose 32-bit timer
- 1x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x temperature sensor
- 1x true random number generator (TRNG)

Packaging

- QFN32 package, 4 x 4 mm

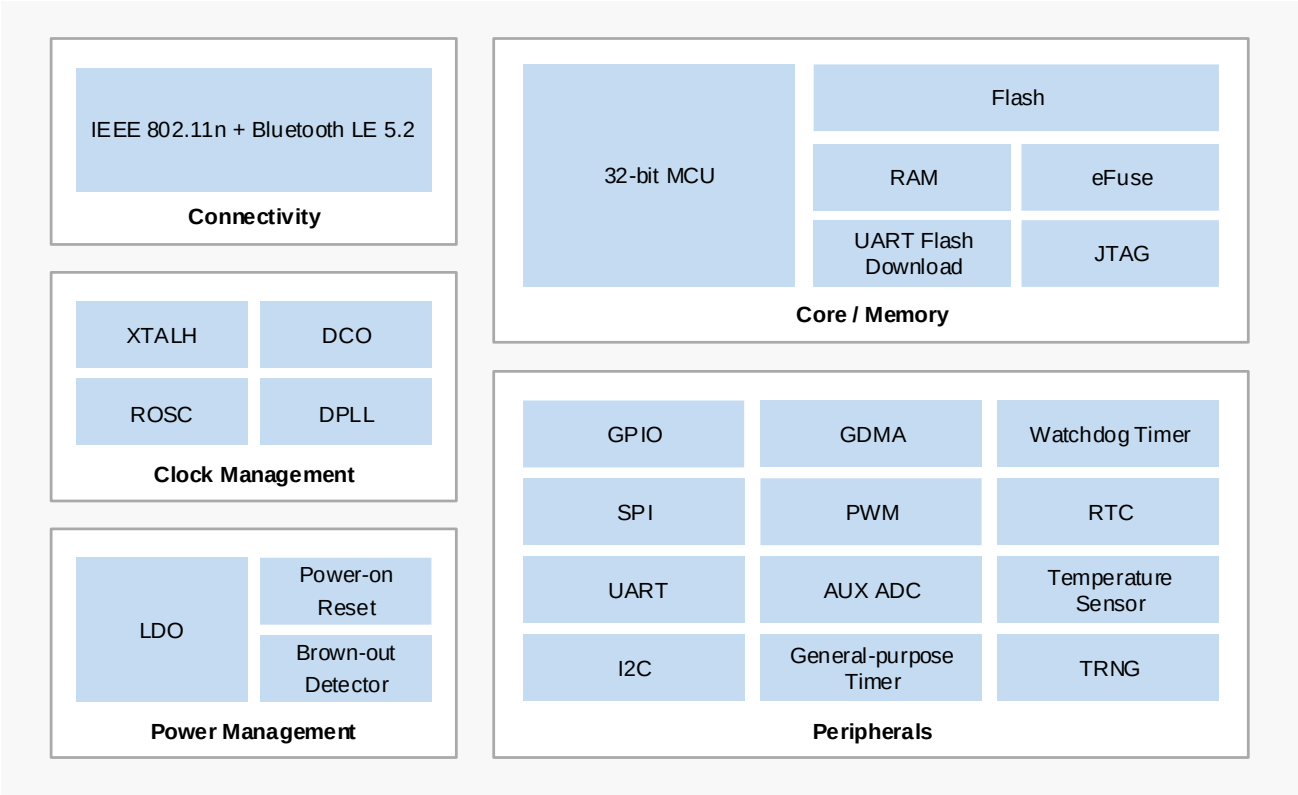
2. Overview

The TG7200C is a highly-integrated single-chip Wi-Fi 802.11n and Bluetooth 5.2 Low Energy (LE) combo solution designed for applications that require low power consumption and compact size. The integration of a powerful 32-bit MCU and a comprehensive set of peripherals and interfaces makes the TG7200C ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and process technology, the TG7200C delivers high integration and minimal power consumption in extremely small packages for smart lighting, smart home, positioning, and other advanced IoT applications.

Figure 2-1 shows the general block diagram of TG7200C.

Figure 2-1 TG7200C Block Diagram



3. Pin Descriptions

The TG7200C provides WLAN and Bluetooth LE functionality in a 4 x 4 mm, 32-pin QFN package. Figure 3-1 shows the pin assignments of the QFN32 package.

Figure 3-1 QFN32 Pin Assignments

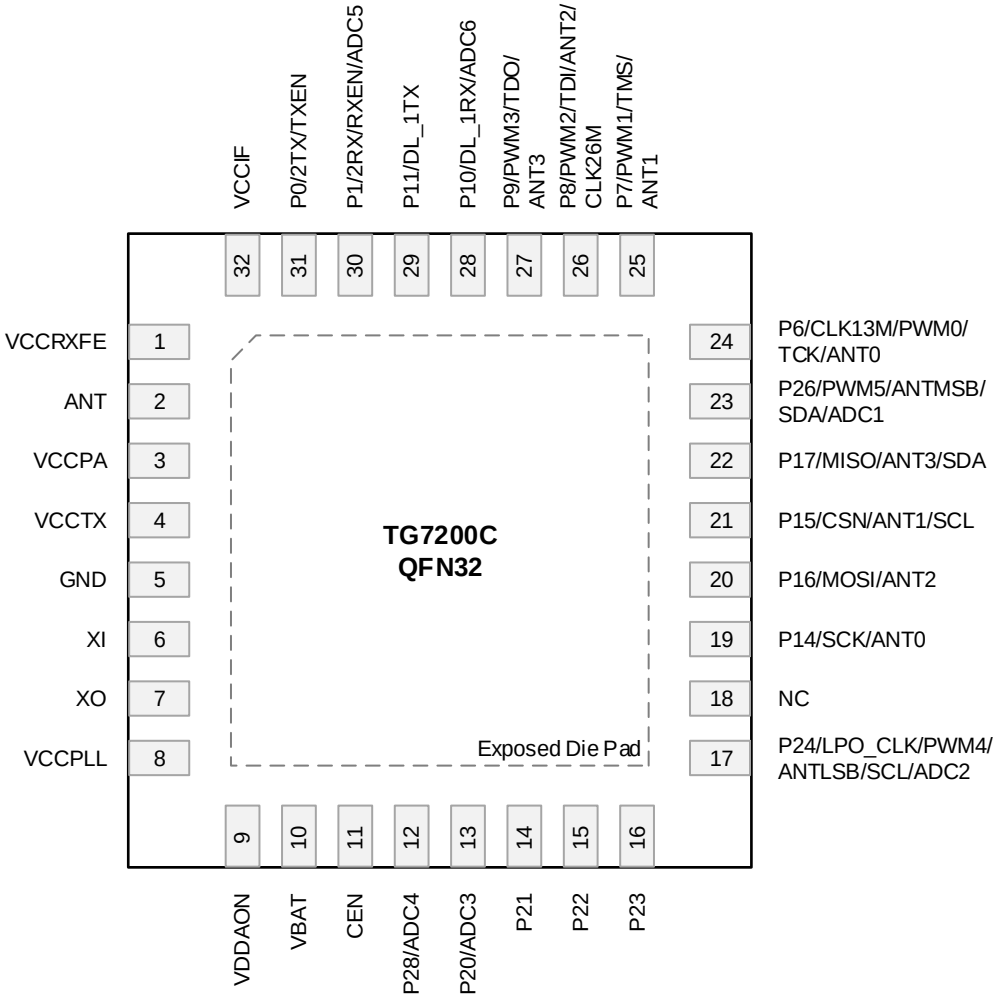


Table 3-1 shows the pin descriptions of the QFN32 package.

Table 3-1 QFN32 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VCCRXFE	-	Analog input	RF receiver power supply
2	ANT	-	RF	2.4 GHz RF signal port

Pin #	Name	I/O	Type	Description
3	VCCPA	-	Analog input	RF PA power supply
4	VCCTX	-	Analog input	RF Transmitter power supply
5	GND	-	GND	Ground
6	XI	-	Analog input	26 MHz crystal input
7	XO	-	Analog output	26 MHz crystal output
8	VCCPLL	-	Analog input	RF PLL power supply
9	VDDAON	-	Analog output	Always-on digital LDO output
10	VBAT	-	Analog input	Chip power supply
11	CEN	-	Analog input	Chip enable, active high
12	P28/ADC4	I/O	Digital/Analog	• GPIO28 • ADC4
13	P20/ADC3	I/O	Digital/Analog	• GPIO20 • ADC3
14	P21	I/O	Digital	GPIO21
15	P22	I/O	Digital	GPIO22
16	P23	I/O	Digital	GPIO23
17	P24/LPO_CLK/PWM4/ANTLSB /SCL/ADC2	I/O	Digital/Analog	• GPIO24 • 32 kHz clock output • PWM4 (differential with PWM5) • Bluetooth LE antenna select (LSB) • I2C: SCL • ADC2
18	NC	-	NC	No connect
19	P14/SCK/ANT0	I/O	Digital	• GPIO14 • SPI: SCK • Bluetooth LE antenna select 0
20	P16/MOSI/ANT2	I/O	Digital	• GPIO16 • SPI: MOSI • Bluetooth LE antenna select 2
21	P15/CSN/ANT1/SCL	I/O	Digital	• GPIO15

Pin #	Name	I/O	Type	Description
				• SPI: CSN • Bluetooth LE antenna select 1 • I2C: SCL
22	P17/MISO/ANT3/SDA	I/O	Digital	• GPIO17 • SPI: MISO • Bluetooth LE antenna select 3 • I2C: SDA
23	P26/PWM5/ANTMSB/SDA/ADC1	I/O	Digital/Analog	• GPIO26 • PWM5 (differential with PWM4) • Bluetooth LE antenna select (MSB) • I2C: SDA • ADC1
24	P6/CLK13M/PWM0/TCK/ANT0	I/O	Digital	• GPIO6 • 26 MHz clock output (divide by 1/2/4/8) • PWM0 (differential with PWM1) • JTAG: TCK • Bluetooth LE antenna select 0
25	P7/PWM1/TMS/ANT1	I/O	Digital	• GPIO7 • PWM1 (differential with PWM0) • JTAG: TMS • Bluetooth LE antenna select 1
26	P8/PWM2/TDI/ANT2/CLK26M	I/O	Digital	• GPIO8 • PWM2 (differential with PWM3) • JTAG: TDI • Bluetooth LE antenna select 2 • 26 MHz clock output
27	P9/PWM3/TDO/ANT3	I/O	Digital	• GPIO9 • PWM3 (differential with PWM2) • JTAG: TDO • Bluetooth LE antenna select 3
28	P10/DL_1RX/ADC6	I/O	Digital/Analog	• GPIO10 • UART1: RX (Flash download support) • ADC6

Pin #	Name	I/O	Type	Description
29	P11/DL_1TX	I/O	Digital	• GPIO11 • UART1: TX (Flash download support)
30	P1/2RX/RXEN/ADC5	I/O	Digital/Analog	• GPIO1 • UART2: RX • RX enable • ADC5
31	P0/2TX/TXEN	I/O	Digital	• GPIO0 • UART2: TX • TX enable
32	VCCIF	-	Analog input	IF power supply
Die pad	GND_SLUG	-	GND	Ground

4. Functional Description

4.1 WLAN/Bluetooth Transceiver

The TG7200C integrates a high-performance WLAN/Bluetooth transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended input and converts the amplified signal into a differential output for a better noise and linearity trade-off. On the transmit side, the differential outputs of the power amplifier (PA) are combined and converted to single-ended outputs using the on-chip balun, enabling transmit and receive operations with only one ANT pin connected to the antenna. The communication range can be extended by configuring GPIO0 and GPIO1 as TXEN and RXEN function to control external PA and LNA. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Power Management

4.2.1 Power Modes

The TG7200C supports four low-power modes except active mode, namely shutdown mode, deep sleep mode, low-voltage sleep mode, and normal sleep mode, where shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are powered off. A high level on the CEN pin will take the system to active mode.

Deep Sleep Mode: All circuits are powered off except the always-on (AON) logic. A GPIO interrupt or an RTC interrupt can power up the system again. Retention registers can keep their contents.

Low-voltage Sleep Mode: The MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, which results in a much lower current. A GPIO interrupt or an RTC interrupt can bring the system back to active mode with normal voltage.

Normal Sleep Mode: The MCU stops running, and all peripheral interrupts can resume the MCU.

Active Mode: The MCU is active, and all peripherals are available.

4.2.2 Power-up Sequence

Figure 4-1 shows the power-up sequence of TG7200C.

Figure 4-1 TG7200C Power-up Sequence

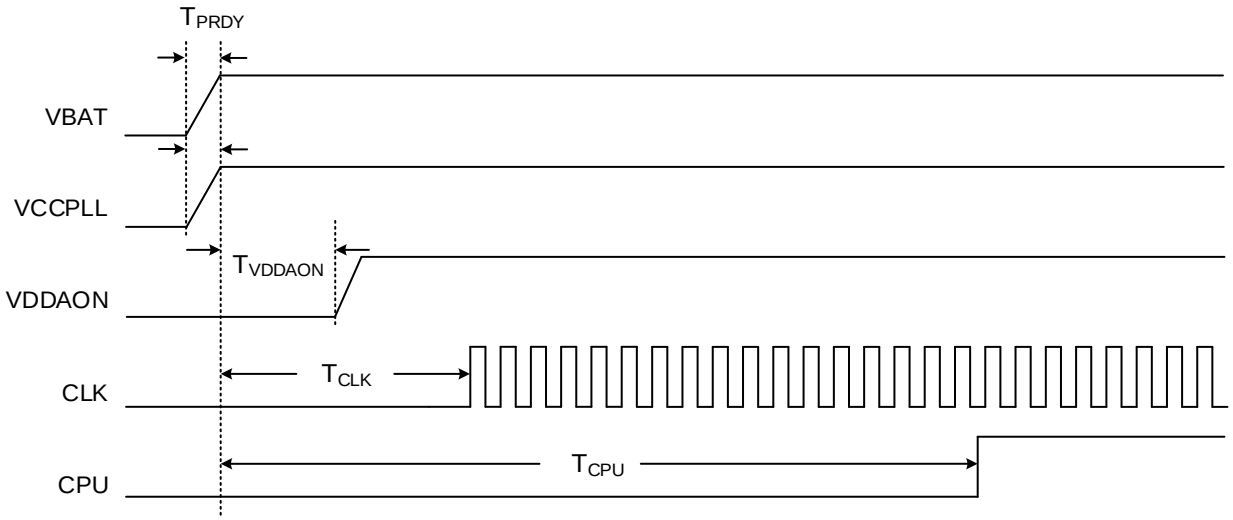


Table 4-1 Timing Parameters of TG7200C Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
T_{PRDY}	VBAT ready time	-	0.5	1.5	ms
T_{VDDAON}	Always-on digital LDO output ready time	-	0.5	1.5	ms
T_{CLK}	26 MHz clock stable time	-	3	5	ms
T_{CPU}	Application ready time	60	70	-	ms

4.3 Clock Management

The primary clock sources available in the TG7200C are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator (XTALH)
  - 26–160 MHz internal digitally controlled oscillator (DCO), about ±2% variation after calibration
  - 480 MHz digital PLL (DPLL)
- Low-frequency clock
  - 32 kHz internal ring oscillator (ROSC), about ±2% variation after calibration

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz clock signal derived from 26 MHz crystal oscillator

- 32 kHz internal oscillator ROSC

The clock selection options for MCU and peripherals are listed as follows.

Table 4-2 Clock Selection

MCU and Peripherals	XTALH	DCO	DPLL	LPO_CLK
MCU	√	√	√	√
FLASH controller	√	√	√	
SPI	√	√		
UART1	√	√		
UART2	√	√		
I2C	√	√		
PWM	√	√		√
AUX ADC	√	√		
TIMG1	√			
TIMG2				√
Watchdog timer				√
RTC				√

The TG7200C also has clock output capability to output clock signals to external components. GPIOs can output the following clock signals:

- LPO_CLK: low-power LPO_CLK clock
- CLK13M: clock derived from high-frequency crystal clock (factor 1/2/4/8)
- CLK26M: high-frequency crystal clock, generally 26 MHz

4.4 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, software reset, and wake-up from shutdown mode or deep sleep mode.

System power-on and watchdog resets have the same reset effect on major blocks, except for the always-on logic. Any of these two resets can reset the whole chip to its initial state. The always-on logic has a 32-bit timer and 16-bit retention registers, which can only be reset to initial values by a system power-on reset. The watchdog reset can also reset the 32-bit timer of the always-on logic.

Wake-up from either shutdown mode or deep sleep mode will power on digital from power-down mode, which triggers the whole system reset procedure.

4.5 General-purpose I/Os (GPIO)

The TG7200C has up to 19 GPIOs, which can be configured as either input or output. Most GPIOs are shared with alternate functions.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.6 SPI Interface (SPI)

The TG7200C integrates an SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 30 MHz in master mode and 20 MHz in slave mode.

The SPI interface supports the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- A 64-depth RX FIFO and a 64-depth TX FIFO with DMA capability

4.7 UART Interface (UART)

The TG7200C includes two universal asynchronous receiver/transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 6 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)

- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Flash download (UART1)

4.8 I2C Interface (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The TG7200C embeds an I2C interface, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection

4.9 GDMA Controller (GDMA)

The TG7200C has a general-purpose DMA controller (GDMA) with six DMA channels to unload CPU activity. The six channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). It allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The peripherals with DMA capabilities on the TG7200C includes UART1, UART2, and SPI.

4.10 PWM

The TG7200C has three 32-bit PWM pairs labeled PWM0/1, PWM2/3, and PWM4/5. Each PWM pair consists of two 32-bit up counters driven by an 8-bit programmable prescaler.

Each channel can work independently (arbitrary waveform configuration), or two channels can be paired (waveforms completely opposite, timing aligned).

When any of the six PWM pins, GPIO6, GPIO7, GPIO8, GPIO9, GPIO24, and GPIO28 is configured as PWM output, the output source can be select from any of the six PWM channels.

The PWM features are listed here:

- 32-bit up counter
- The counter increases in one direction and automatically continues counting from 0 when it overflows to the maximum value.
- Fixed PWM base frequency with 8-bit programmable prescaler (factor between 1 and 256)
- Six channels, each supports four modes:
  - PWM mode
  - Timer mode
  - Counter mode
  - Capture mode
- Each channel can be enabled individually, and the mode of each channel can be configured individually.
- Configurable PWM period and duty cycle for each PWM channel
- Capable of continuously counting between two rising edges, two falling edges, or any two edges in Capture mode
- Real-time count value can be read in Timer mode.

4.11 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 10-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC has the following features:

- Programmable sample rate from 5 kHz to 26 MHz
- 10-bit resolution
- Up to six external analog input channels: ADC1/2/3/4/5/6
- Four internal dedicated channels:
  - VBAT monitoring channel (VBAT/2), connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - TSSIO, connected to ADC8
  - Internal debug channel, connected to ADC9
- Conversion modes:

- One-shot mode
- Software control mode
- Continuous mode

4.12 Timer Group (TIMG)

The TG7200C includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

4.13 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect and recover from failures or malfunctions. It triggers a reset on expiry of a specified time period.

The watchdog timer runs on the 32 kHz LPO_CLK clock and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

4.14 Real-time Counter (RTC)

The real-time counter (RTC) is a 32-bit counter that can be used as a wake-up source to wake up the system from low-voltage sleep or deep sleep mode. The RTC runs on the ROSC, and it can keep running even when the system is in low-voltage sleep or deep sleep mode.

4.15 Temperature Sensor

The TG7200C integrates an on-chip temperature sensor. The temperature sensor can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read by the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

4.16 True Random Number Generator (TRNG)

The random number generator module generates true, nondeterministic random numbers based on thermal noise for the purpose of creating keys, initialization vectors, and nonces needed for cryptographic operations.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Battery regulator supply voltage	-0.3	3.6	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	℃

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001-2017	ANT pin	±2000	V
		VCCPA/VCCTX/XI pins	±3000	V
		Other pins	±4000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002-2018	All pins	±1000	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Battery/regulator supply voltage	2.7	-	3.6	V
VCCIF	Supply voltage for IF	2.7	-	3.6	V
VCCRXFE	Supply voltage for RX	2.7	-	3.6	V
VCCPA	Supply voltage for PA	2.7	-	3.6	V
VCCTX	Supply voltage for TX	2.7	-	3.6	V
VCCPLL	Supply voltage for RF PLL	2.7	-	3.6	V

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAON	Always-on digital LDO output voltage	0.5	0.9	1.0	V

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VBAT	-	VBAT + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VBAT	V
VOH	High-level output voltage	-	0.9 VBAT	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VBAT	V
I_{DRV}	I/O output drive strength	-	5	-	20	mA
R_{PU}	Weak pull-up resistor	-	-	48	-	kΩ
R_{PD}	Weak pull-down resistor	-	-	48	-	kΩ

5.5 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDAON	Always-on digital LDO output voltage	0.5	0.9	1.0	V
Load current	-	-	-	50	mA

5.6 26 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal Frequency	-	-	26	-	MHz
ΔF/F0	Frequency tolerance	25 ℃	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 ℃ crystal	-20	-	+20	ppm
		-30 to 85 ℃ crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7.3	9	pF
TS	Trim sensitivity	-40 to 105 ℃ crystal	-	32	-	ppm/pF
		-30 to 85 ℃ crystal	-	17	-	ppm/pF

5.7 Current Consumption

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11 Mbps DSSS	-	30	-	mA
	54 Mbps OFDM	-	33	-	mA
	MCS7, HT20	-	33	-	mA
TX current	11 Mbps DSSS @ 17 dBm	-	265	-	mA
	54 Mbps OFDM @ 15 dBm	-	230	-	mA
	MCS7, HT20 @ 14 dBm	-	220	-	mA
Sleep Mode					
Normal sleep	-	-	300	-	µA
Low-voltage sleep	-	-	75	-	µA
Deep sleep	-	-	10	-	µA
Shutdown Mode					
Shutdown	-	-	0.5	-	µA

5.8 WLAN Receiver RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	-	-99	-	dBm
	2 Mbps DSSS	-	-96	-	dBm
	5.5 Mbps DSSS	-	-94	-	dBm
	11 Mbps DSSS	-	-90	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM		-	-92	-	dBm
	9 Mbps OFDM		-	-92	-	dBm
	12 Mbps OFDM		-	-91	-	dBm
	18 Mbps OFDM		-	-89	-	dBm
	24 Mbps OFDM		-	-86	-	dBm
	36 Mbps OFDM		-	-82	-	dBm
	48 Mbps OFDM		-	-78	-	dBm
	54 Mbps OFDM		-	-76	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU)	MCS0		-	-92	-	dBm
	MCS1		-	-90	-	dBm
	MCS2		-	-87	-	dBm
	MCS3		-	-84	-	dBm
	MCS4		-	-81	-	dBm
	MCS5		-	-77	-	dBm
	MCS6		-	-75	-	dBm
	MCS7		-	-74	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)		-	-	10	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)		-	-	10	dBm
	11g: 6–54 Mbps (10% PER, 1000 octets)		-	-	5	dBm
	11n: MCS0–7 (10% PER, 4096 octets)		-	-	2	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	51	-	dB
	2 Mbps DSSS	-74 dBm	-	48	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
Adjacent channel (±25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	42	-	dB
	11 Mbps DSSS	-70 dBm	-	37	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g (10% PER for 1000 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	42	-	dB
	54 Mbps OFDM	-62 dBm	-	30	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	MCS0	-79 dBm	-	42	-	dB
	MCS7	-61 dBm	-	24	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-	-60	dBm
	> 1 GHz		-	-	-60	dBm

5.9 WLAN Transmitter RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	19	-	dBm
	11 Mbps DSSS	-	19	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	20	-	dBm
	54 Mbps OFDM	-	17	-	dBm
TX power - IEEE 802.11n (EVM compliant)	MCS0	-	19	-	dBm
	MCS7	-	16	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
Harmonic Level						
Harmonic level (at maximum output power)	4.8–5.0 GHz	2nd harmonic	-	-	-45	dBm
	7.2–7.5 GHz	3rd harmonic	-	-	-50	dBm
Spurious Emissions						
Spurious emissions (at maximum output power)	< 1 GHz		-	-	-50	dBm
	> 1 GHz		-	-	-43	dBm

5.10 Bluetooth LE Receiver RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-98	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 1 MHz adjacent channel	-	-	0	-	dB
C/I -1 MHz adjacent channel	-	-	-1	-	dB
C/I 2 MHz adjacent channel	-	-	-29	-	dB
C/I -2 MHz adjacent channel	-	-	-30	-	dB
C/I 3 MHz adjacent channel	-	-	-30	-	dB
C/I -3 MHz adjacent channel	-	-	-29	-	dB
C/I > 3 MHz adjacent channel	-	-	-29	-	dB
C/I < -3 MHz adjacent channel	-	-	-30	-	dB
Out-of-band blocking	30–2000 MHz	-	-27	-	dBm
	2003–2399 MHz	-	-33	-	dBm
	2484–2997 MHz	-	-32	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	3000 MHz–12.75 GHz	-	-10	-	dBm
Intermodulation	-	-	-38	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-95	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 2 MHz adjacent channel	-	-	0	-	dB
C/I -2 MHz adjacent channel	-	-	-2	-	dB
C/I 4 MHz adjacent channel	-	-	-29	-	dB
C/I -4 MHz adjacent channel	-	-	-29	-	dB
C/I 6 MHz adjacent channel	-	-	-29	-	dB
C/I -6 MHz adjacent channel	-	-	-29	-	dB
C/I > 6 MHz adjacent channel	-	-	-30	-	dB
C/I < -6 MHz adjacent channel	-	-	-29	-	dB
Out-of-band blocking	30–2000 MHz	-	-28	-	dBm
	2003–2399 MHz	-	-33	-	dBm
	2484–2997 MHz	-	-29	-	dBm
	3000 MHz–12.75 GHz	-	-5	-	dBm
Intermodulation	-	-	-38	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	-104	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	1	-	dB
C/I 1 MHz adjacent channel	-	-	-3	-	dB
C/I -1 MHz adjacent channel	-	-	-4	-	dB
C/I 2 MHz adjacent channel	-	-	-31	-	dB
C/I -2 MHz adjacent channel	-	-	-34	-	dB
C/I 3 MHz adjacent channel	-	-	-34	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I -3 MHz adjacent channel	-	-	-41	-	dB
C/I > 3 MHz adjacent channel	-	-	-41	-	dB
C/I < -3 MHz adjacent channel	-	-	-41	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	-101	-	dBm
Maximum input level	30.8% PER	0	-	-	dBm
C/I co-channel	-	-	4	-	dB
C/I 1 MHz adjacent channel	-	-	-2	-	dB
C/I -1 MHz adjacent channel	-	-	-3	-	dB
C/I 2 MHz adjacent channel	-	-	-31	-	dB
C/I -2 MHz adjacent channel	-	-	-33	-	dB
C/I 3 MHz adjacent channel	-	-	-32	-	dB
C/I -3 MHz adjacent channel	-	-	-34	-	dB
C/I > 3 MHz adjacent channel	-	-	-34	-	dB
C/I < -3 MHz adjacent channel	-	-	-34	-	dB

5.11 Bluetooth LE Transmitter RF Characteristics

Measured with T = 25 °C, VBAT = 3.0 V unless otherwise stated.

Parameter		Condition	Min.	Typ.	Max.	Unit
General						
Frequency range		-	2402	-	2480	MHz
TX power		-	6	8	10	dBm
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-49	-	dBm
	±3 MHz offset	-	-	-50	-	dBm
	> ±3 MHz offset	-	-	-51	-	dBm
Modulation	Δf1avg	-	-	262	-	kHz

Parameter		Condition	Min.	Typ.	Max.	Unit
characteristics	Δf2max	-	-	250	-	kHz
	Δf2avg/Δf1avg	-	-	0.9	-	-
Carrier frequency offset and drift	Max $\lvert f_n \rvert$ n = 0, 1, 2, 3…k	-	-	8	-	kHz
	Max $\lvert f_0 - f_n \rvert$ n = 2, 3, 4…k	-	-	1.5	-	kHz
	$\lvert f_1 - f_0 \rvert$	-	-	0.5	-	kHz
	Max $\lvert f_n - f_{n-5} \rvert$ n = 6, 7, 8…k	-	-	1.3	-	kHz/50 µs
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	-52	-	dBm
	±5 MHz offset	-	-	-52	-	dBm
	> ±5 MHz offset	-	-	-53	-	dBm
Modulation characteristics	Δf1avg	-	-	522	-	kHz
	Δf2max	-	-	502	-	kHz
	Δf2avg/Δf1avg	-	-	0.9	-	-
Carrier frequency offset and drift	Max $\lvert f_n \rvert$ n = 0, 1, 2, 3…k	-	-	10	-	kHz
	Max $\lvert f_0 - f_n \rvert$ n = 2, 3, 4…k	-	-	1.2	-	kHz
	$\lvert f_1 - f_0 \rvert$	-	-	0.5	-	kHz
	Max $\lvert f_n - f_{n-5} \rvert$ n = 6, 7, 8…k	-	-	0.9	-	kHz/50 µs
Bluetooth LE 125 kbps						
In-band emissions	±2 MHz offset	-	-	-49	-	dBm
	±3 MHz offset	-	-	-50	-	dBm
	> ±3 MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf1avg	-	-	261	-	kHz
	Δf1max	-	-	245	-	kHz
Carrier frequency offset and drift	Max $\lvert f_n \rvert$ n = 0, 1, 2, 3…k	-	-	10	-	kHz
	Max $\lvert f_0 - f_n \rvert$ n = 1, 2, 3…k	-	-	1	-	kHz
	$\lvert f_0 - f_3 \rvert$	-	-	1	-	kHz

Parameter		Condition	Min.	Typ.	Max.	Unit
	$\lvert f_n - f_{n-3} \rvert$ n = 7, 8, 9…k	-	-	1	-	kHz/48 µs
Bluetooth LE 500 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-48	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm

5.12 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	-	-	1.86	MHz
Conversion time	-	14	-	-	Cycle
V_{REF}	Internal	0.8	1.8	-	V
	External	-	VBAT/2	-	V
Input voltage range	-	0	-	V_{REF}*2	V
Input impedance	-	100	-	-	MΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-1	-	0.5	LSB
INL	-	-2	-	2	LSB
ENOB	-	-	9.2	-	Bit
SNDR	-	-	57	-	dB
SFDR	-	-	61.4	-	dB
$T_{STARTUP}$	-	-	5	-	µs
Current consumption	-	-	200	-	µA

6. Package Information

Figure 6-1 QFN32 4 x 4 mm Package Outline

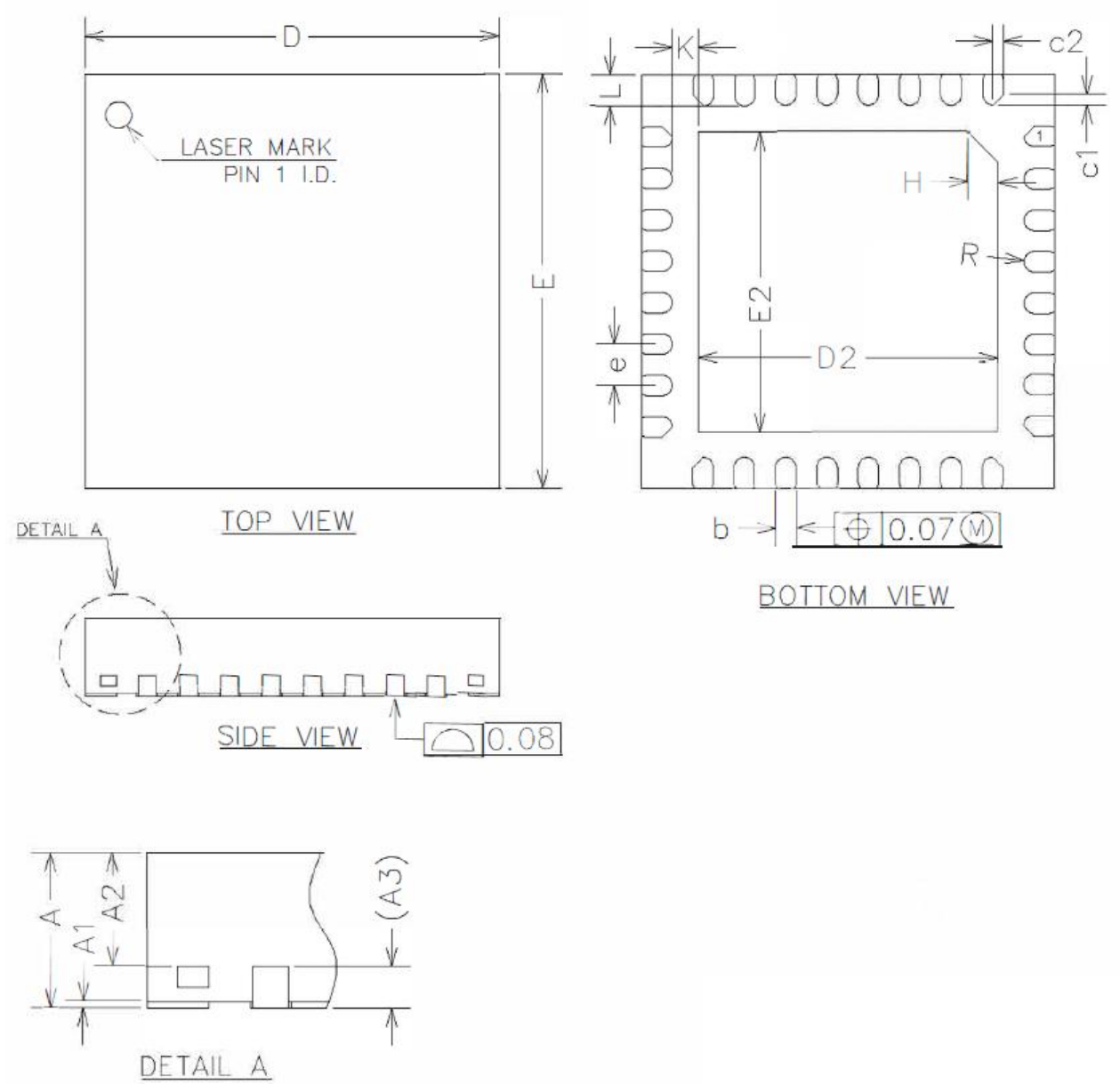
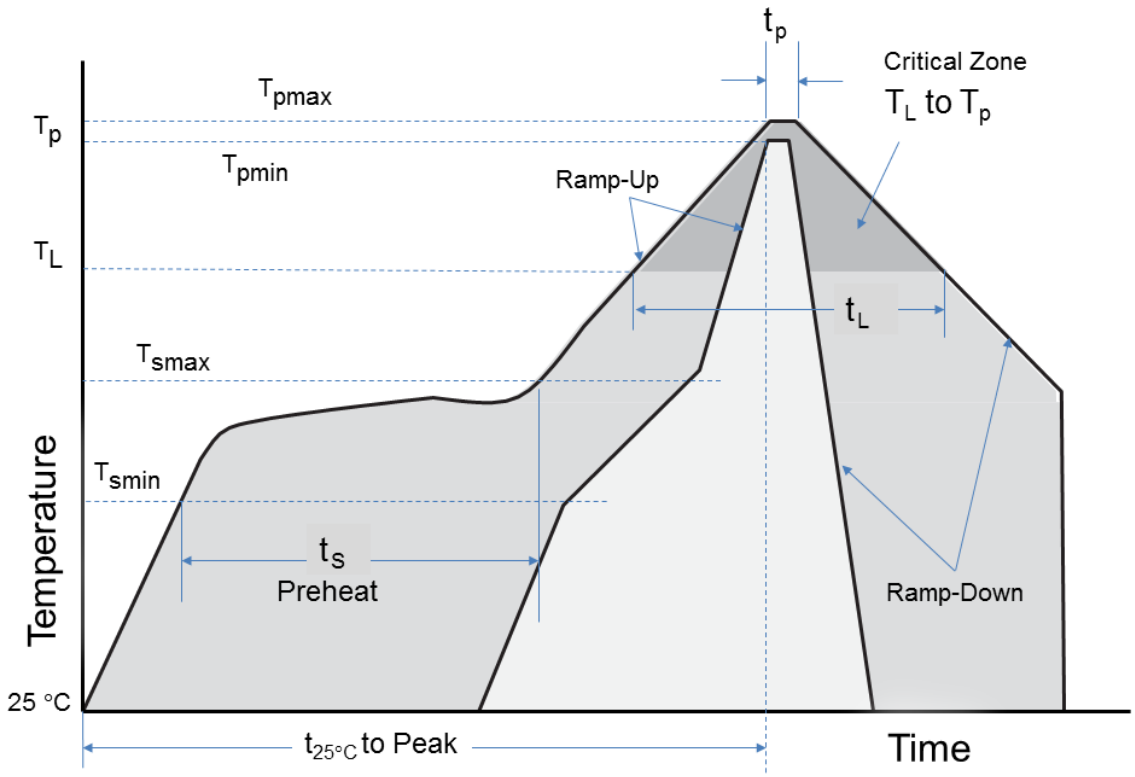


Table 6-1 QFN32 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30 REF		
K	0.25 REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/s max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 s to 40 s

Profile Feature	Specification
Ramp-down rate	6 ℃/s max.
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Table 8-1 Ordering Information

Ordering Code	Package	SiP[a] Flash	Ambient Temp	Packing	Minimum Ordering Qty (MOQ)
TG7200CQH321	4 mm x 4 mm QFN32	2 MB	-40 to +105 ℃	Tape and Reel	3000

a. A system in a package (SiP) refers to Flash enclosed in the package.

Revision History

Version	Date	Description
1.0	2023/10/18	Initial release